Amendments to the Claims

1. (currently amended) A method of processing interrupts, the method comprising:

detecting an indicator of an interrupt signal from an expansion device residing on an expansion bus, wherein the detecting occurs at a local device on a local bus;

transferring data related to the interrupt signal from the device across the expansion bus to a local memory; and

processing the data related to the interrupt signal.

2. (original) The method of claim 1, detecting an indicator of an interrupt further comprising receiving an interrupt at a central processor.

3. (original) The method of claim 1, detecting an indicator of an interrupt further comprising receiving an interrupt on an interrupt line to a direct memory access controller.

4. (original) The method of claim 1, detecting an indicator of an interrupt further comprising using a direct memory access controller to detect a voltage change on an interrupt line.

5. (original) The method of claim 1, transferring data further comprising using a direct memory access controller to transfer data from any expansion devices that generated interrupt signals.

6. (original) The method of claim 1, transferring data further comprising using a direct memory access controller to transfer data from expansion device to local memory and generating an interrupt to a central processor.

7. (original) The method of claim 1, transferring data further comprising updating a memory access monitor bit in a memory access monitor status register.

8. (currently amended) A method of processing interrupts, the method comprising:

detecting interrupt signals at a processor;

determining if the interrupt signals are from local devices or expansion devices that reside on an expansion bus;

directing a direct memory access controller residing on a local bus with the processor to read a status register for any expansion devices that have generated interrupt signals;

processing any interrupt signals from local devices; and

processing any interrupt signals from devices located across the expansion bus.

9. (original) The method of claim 8, detecting interrupt signals further comprising receiving interrupt signals at a central processor.

10. (original) The method of claim 8, determining further comprising determining that the interrupt signals are from local devices and any expansion devices further comprise no expansion devices.

11. (original) The method of claim 8, determining further comprising determining that the interrupt signals are from expansion devices and directing a memory access controller further comprises directing a memory access controller to process a second interrupt while processing a first interrupt.

12. (currently amended) A method of processing interrupts, the method comprising:

detecting an update to a descriptor memory at a direct memory access controller local to a central processor;

updating a register corresponding to the descriptor memory in a local status register;

generating an interrupt to a the central processor;

identifying a device generating the update; and

performing a task associated with the descriptor memory.

13. (original) The method of claim 12, detecting an update to a descriptor memory further comprising detecting an update to a descriptor memory using a memory access monitor.

14. (original) The method of claim 12, performing a task further comprising transmitting a packet.

15. (original) The method of claim 12, performing a task further comprising determining a next hop for a received packet.

16. (currently amended) A method of processing interrupts, the method comprising:

detecting an interrupt at a direct memory access controller residing on a local bus with a central processor from a device located across an expansion bus from a the central processor;

transferring data from the device to a local memory residing on the local bus; and

generating an interrupt signal to the central processor when transfer is complete.

17. (original) The method of claim 16, detecting an interrupt further comprising receiving an interrupt on an interrupt line to a direct memory access controller.

18. (original) The method of claim 16, detecting an interrupt further comprising using a direct memory access controller to detect a voltage change on an interrupt line.

19. (currently amended) A device, comprising:

a central processor having at least one direct memory access controller local to the processor;

an expansion bus;

at least one expansion device in communication with the central processor through the expansion bus; and

at least one interrupt signal line electrically coupled between the direct memory access controller and the expansion bus.

20. (currently amended) The device of claim 19, at least one interrupt signal line further comprising at least one interrupt signal line directly connected to the direct memory access controller.

21. (original) The device of claim 19, at least one interrupt signal line further comprising a detection line electrically coupled between a central interrupt signal line and a direct memory access controller.

22. (currently amended) A device, comprising:

a central processor having at least one direct memory access controller local to the central processor;

an expansion bus;

at least one expansion device in communication with the central processor through the expansion bus; and

a memory access monitor residing on a local bus with the central processor electrically coupled to a memory to detect updates to the memory made by an expansion device.

23. (original) The device of claim 22, the memory access monitor further to detect an update to a receive descriptor memory.

24. (original) The device of claim 22, the memory access monitor further to detect an update to a transmission descriptor memory.

25. (original) The device of claim 22, the memory access monitor being implemented inside a system controller.

26. (original) The device of claim 22, the memory access monitor being implemented in software executed by a system controller.

27. (canceled)

28. (currently amended) A device, comprising:

means for detecting an interrupt indicator from an expansion device on an expansion bus at a device on a local bus;

means for transferring data related to the interrupt signal from the device to a local memory on the local bus; and

means for processing the data related to the interrupt.

29. (canceled)

30. (currently amended) A device, comprising:

means for detecting interrupt signals;

means for determining sources of the interrupt signals;

means for directing a direct memory access controller local to a central processor to read a status register for any expansion devices that have generated interrupt signals;

means for processing any interrupt signals from local devices; and

processing any interrupt signals from expansion devices.

31. (canceled)

32. (currently amended) A device, comprising:

means for detecting an update to a descriptor memory, the means being local to a central processor;

means for updating a register corresponding to the descriptor memory in a local status register;

means for interrupting ~~a~~ the central processor;

means for identifying a device generating the update; and

means for performing a task associated with the update.

33. (currently amended) A device, comprising:

means for detecting an interrupt at a direct memory access controller local to a central processor from an expansion device on an expansion bus;

means for transferring data from the device to a local memory; and

means generating an interrupt signal to the central processor when transfer is complete.